CCD211
244x190 Element Array
CCD221
488x380 Element Array

CCD Imaging

Description

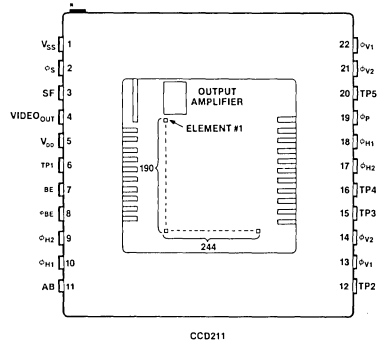
The CCD211 and CCD221 are 244x190 and 488x380-element solid-state charge-coupled device area image sensors which are intended for use as high-resolution detectors in a variety of scientific and industrial optical instrumentation systems. The CCD211 is organized as a matrix array of 244 horizontal lines by 190 vertical columns and the CCD221, 488 horizontal lines by 380 vertical columns of charge-coupled photoelements. The dimensions of the 46,360 photoelements of the CCD211 and the 185,440 photoelements of the CCD221 are 12 μm horizontally by 18 μm vertically. The photoelements are precisely positioned on 30 μm horizontal centers and 18 μm vertical centers. The CCD211 has an image sensing area of 4.4 by 5.7 mm, with a diagonal dimension of 7.2 mm and the CCD221 has an active area of 8.8 by 11.4 mm, with a diagonal of 14.4 mm.

The low noise performance of the buried channel CCD structure can provide excellent low-light-level capabilities when cooled. The geometric accuracy of the device structure, combined with a video readout which is controlled by digital clock signals, allows the signal output from each photo-element to be precisely identified for easy realization of computer-based image processing systems. The devices can be used in video cameras that require low power, small size, high sensitivity, high reliability and rugged construction.

- **46,360/185,440* SENSING ELEMENTS ON A SINGLE CHIP**
- **AVAILABLE HORIZONTAL RESOLUTION: 190/380 ELEMENTS PER LINE**
- **AVAILABLE VERTICAL RESOLUTION: 244/488 LINES**
- **NO LAG, NO GEOMETRIC DISTORTION**
- **A GAMMA OF UNITY**
- **HIGH DYNAMIC RANGE—TYPICALLY: 1,000:1 at 25°C (EXCLUDING DARK SIGNAL NON-UNIFORMITY)**
- **LOW LIGHT LEVEL CAPABILITY, LOW NOISE EQUIVALENT EXPOSURE**
- **VIDEO DATA RATES UP TO 20 MHz, FRAME RATES TO 360/90 Hz**
- **SAMPLE-AND-HOLD VIDEO OUTPUT**
- **LOW POWER DISSIPATION, SOLID-STATE RELIABILITY AND SMALL SIZE**
- **STANDARD TV ASPECT RATIO (4:3)**
- **CCD221 SATISFIES NTSC RESOLUTION STANDARDS**
- **TWO-PHASE REGISTER CLOCKING**
- **DIGITALLY-CONTROLLED READOUT**

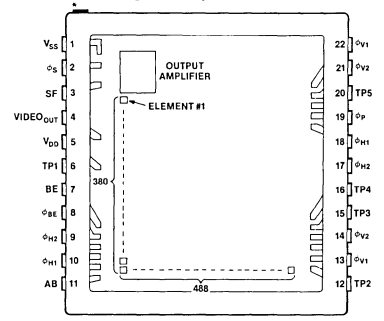
*CCD211 Parameter/CCD221 Parameter

Connection Diagram (Top View)



CCD211

Connection Diagram (Top View)



CCD221

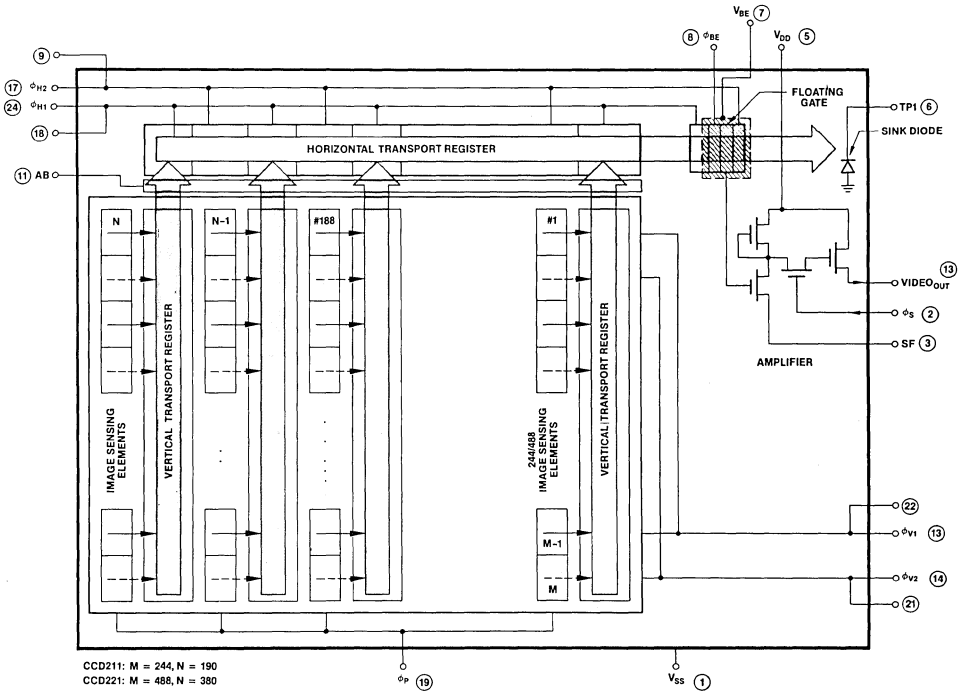
*PIN 1 (V_{SS}) IS DESIGNATED BY A DOT ON SIDE OF PACKAGE

Pin Names

AB	Anti-Blooming Bias (for Column Anti-Blooming)
SF	Floating-Gate Amplifier Source
$VIDEO_{OUT}$	Output Amplifier Source
ϕ_P	Photogate Clock
ϕ_{V1}, ϕ_{V2}	Vertical Transport Clocks
ϕ_{H1}, ϕ_{H2}	Horizontal Transport Clocks
ϕ_{BE}	Bias Electrode Clock
BE	DC Bias Electrode
ϕ_S	Sample-and-Hold Clock
V_{DD}	Output Amplifier Drain
V_{SS}	Substrate (GND)
TP	Test Points

CCD211/CCD221

Block Diagram



Functional Description

The CCD211/221 consist of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements

Image photons pass through a transparent polycrystalline silicon gate structure and are absorbed in the silicon crystal structure creating hole-electron pairs. The resulting photoelectrons are collected in the photosites during the integration period; the amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and the integration period.

Vertical Analog Transport Registers

At the ends of integration periods, the charge packets are transferred out of the array in two sequential fields of 122/244 lines each. When the photogate voltage is lowered, charge packets from odd-numbered photosites (1, 3, 5 . . . 243/487) are transferred to the vertical transport registers at the beginning of readout of an odd field when the ϕ_{V1} clock is HIGH. Clocking ϕ_{V1} and ϕ_{V2} then transports the charge packets up the vertical transport registers, line by line, to the output horizontal transport register. Before the readout of the next even field and when the photogate voltage is again lowered, the ϕ_{V2} clock is held HIGH causing the transfer of the even-numbered photosite charge packets (2, 4, 6 . . . 244/488) to the vertical registers. A minimum of 123/245 vertical clock pulses are required per field to deliver the entire field to the output. The additional clock cycle is required due to

the existence of a non-sensitive anti-blooming line between the horizontal transport register and the top of the vertical columns.

Horizontal Analog Transport Register
The horizontal transport register is a 190/380 element 2-phase register that receives the charge packets from the vertical registers line by line. After each line of information is transferred from the vertical transport registers, it is moved serially to the output amplifier by the complementary horizontal clocks ϕ_{H1} and ϕ_{H2}. A minimum of 195/385 horizontal clock pulses are required to complete transfer of one line of information to the floating-gate amplifier.

Floating-Gate Amplifier
The charge packets from the horizontal transport register are sensed by a floating-gate whose potential changes linearly with the quantity of signal charge and which drives an input MOS transistor. The output signal from this transistor in turn drives the gate of an output n-channel MOS transistor which produces the video output signal at terminal $VIDEO_{OUT}$. The signal is sampled under control of clock ϕ_S through a MOS transistor switch. The resultant video output signal is a sampled-and-held clock-controlled analog signal representing the spatial distribution of the sensor surface exposure.

Sampled Video Output (SEE TIMING DIAGRAM)
The output waveform of the CCD211/221 is shown in detail in the Timing Diagram. Each *frame* (244/488 horizontal lines) is delivered to the output in two sequential *fields* of 122/244 horizontal lines each. Each horizontal line is 190/380-elements long.

The sequence of data comprising each horizontal line is as follows:

1. At the beginning of each line are 4 pre-scan elements which contain no video information, but are representative of the dark current levels in the horizontal register.
2. The output then contains information from 5 elements which are covered with opaque aluminum including:
   A) A peripheral response element containing information representative of the charge generated around the periphery of the device. This element output should be ignored.
   B) Three dark reference cells which contain no video information, but correspond to the true dark current (the sum of register plus photosite currents) of that particular line. These elemental outputs may be used as dark reference levels in post-output dc restoration circuitry.
   C) A peripheral response reduction element which is partially covered by aluminum.
3. Following are the 185/375 elements which contain the true video information (valid pixels) showing the spatial distribution of incident brightness for that line.

Definition of Terms

Charge-Coupled Device — A charge-coupled device is a monolithic silicon structure in which discrete isolated packets of electrical charge are transported from position to position in the semiconductor by sequential clocking of an array of gates. The charge packets are minority carriers (electrons) with respect to the semiconductor substrate.

Photogate Clock ϕ_P — The voltage waveform applied to the photogate to move the accumulated charge from the image sensor elements to the vertical transport registers.

Vertical Transport Clocks ϕ_{V1}, ϕ_{V2} — The two clocks applied to the vertical transport registers to move the charge packets received from the image sensor elements towards the CCD horizontal transport register.

Horizontal Transport Clocks ϕ_{H1}, ϕ_{H2} — The two clocks applied to the horizontal transport register to move the charge packets received from the vertical transport registers towards the floating-gate amplifier.

Floating-Gate Amplifier — The first stage of the on-chip amplifier which develops a signal voltage linearly proportional to the number of electrons contained in each sensed charge packet. The floating-gate is coupled to the charge transport channel exclusively by electrostatic fields for low-noise signal detection.

Sample-and-Hold Clock ϕ_S — The clock applied to the sample-and-hold gate of the amplifier. The sample-and-hold feature can be disabled by connecting ϕ_S to V_{DD}.

Dark Reference — Video output level generated from photoelements covered with opaque metalization. The video output from these elements provides a reference voltage equivalent to sensor operation in the dark.

Dynamic Range — The saturation level output video signal voltage of the sensor divided by the rms noise output of the sensor in the dark. The peak-to-peak random noise output of the device is 4-6 times the rms noise output.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

CCD211/CCD221

Responsivity — The output signal voltage per unit exposure for a specified radiation spectrum. Responsivity equals output voltage divided by exposure.

Photoresponse Shading Non-Uniformity — The difference of the response levels between the most and least sensitive regions under uniform illumination, excluding blemished elements. Shading is measured using a low-pass filter with a cut-off of approximately 10 cycles per picture width in the video output line.

Dark Signal — The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

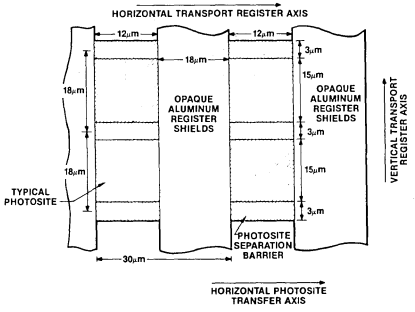
Dark Signal Shading Non-Uniformity — The difference in the dark signal levels between the lowest and highest outputs from non-blemished elements in the dark. Shading is measured using a low-pass filter with a cut-off frequency of approximately 10 cycles per picture width in the video output line.

Saturation Output Voltage — The maximum available useful signal output voltage, measured with respect to the zero reference level.

Integration Time — Two times the time interval between the falling edges of any two successive ϕ_P clock pulses shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — Picture element (photosite — see dimensions figure 9.)

Photosite Dimensions



NOTE: Photosite Separation Barriers are transparent, photosites are optically contiguous along the vertical axis.

Absolute Maximum Ratings

STORAGE TEMPERATURE	−100°C to +100°C
VOLTAGES:	
Pins 3, 4, 5, 6, 11, 15, 20	-0.3V to +16V
Pins 2, 7, 8, 9, 10, 12, 13, 14, 16, 17, 18, 19, 21, 22	−10V to +15V
Pin 1	V_{SS} = 0V

Caution Note

The devices do not have built-in gate protection. It is crucial that static discharge be controlled and minimized. Care must be taken to avoid shorting pin $VIDEO_{OUT}$ to V_{SS} or V_{DD} during operation of the device. Shorting this pin temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

Dirty glass windows on devices cause increased photoresponse non-uniformity. Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

DC Operating Conditions and Characteristics: Devices are tested at nominal conditions except for V_{SF}, V_{BE}, and V_{AB} which are adjusted for individual sensors.

Symbol	Parameter	Range			Unit	Remarks
		Min.	Nom.	Max.		
V_{DD}	DC Supply Voltage	12.0	15.0	16.5	V	
V_{AB}	Anti-Blooming Bias Voltage	6.0	10.0	V_{DD}	V	Note 1
V_{SF}	Source of Floating-Gate Amplifier	4.0	7.0	10.0	V	Note 1
V_{BE}	Bias Electrode	-5.0	0.0		V	Note 1
TP_2, TP_4	Test Points		0.0		V	
TP_1, TP_3, TP_5	Test Points		V_{DD}		V	
I_{DD}	DC Supply (V_{DD}) Current		3.5		mA	T_C = 0°C
I_{SF}	Floating-Gate Amplifier Current		1		μA	T_C = 0°C

Clock Conditions

Symbol	Parameter	Range			Unit	Remarks
		Min.	Nom.	Max.		
$V_{\phi PL}$	Photogate Clock LOW	−6.0	0.0		V	Note 2, 10
$V_{\phi PH}$	Photogate Clock HIGH	3.0	5.0	7.0	V	Note 2
$V_{\phi BEL}$	Bias Electrode of FGA Clock LOW	−3.0	0.0	0.0	V	
$V_{\phi BEH}$	Bias Electrode of FGA Clock HIGH	0.0	5.0	7.0	V	Note 1
$V_{\phi H1L}$ $V_{\phi H2L}$	Horizontal Transport Clock LOW	−5.0	0.0	0.0	V	Note 3
$V_{\phi H1H}$ $V_{\phi H2H}$	Horizontal Transport Clock HIGH	5.0	9.0	12.0	V	Note 1, 3
$V_{\phi V1L}$ $V_{\phi V2L}$	Vertical Transport Clock Low	−6.0	0.0	0.0	V	Note 2, 10
$V_{\phi V1H}$ $V_{\phi V2H}$	Vertical Transport Clock HIGH	5.0	9.0	12.0	V	Note 4
$V_{\phi SL}$	Sample-and-Hold Clock LOW	−3.0	0.0	0.0		
$V_{\phi SH}$	Sample-and-Hold Clock HIGH	3.0	5.0	7.0	V	
$f_{\phi H1}$ $f_{\phi H2}$	Max Horizontal Transport Clock Frequency	7.2		20.0	MHz	Note 5

CCD211/CCD221

Performance Specifications: Standard Test conditions are TV format data output at a 30 Hz frame rate, 60 Hz field rate, 15.75 kHz line rate, 7.16 MHz pixel rate, T_C = 0°C. Light source is 2854°K incandescent with 2.0 mm thick Schott BG-38 IR reject filter.

Symbol	Parameter	CCD211/221 Min	CCD211/221 Typ	CCD211/221 Max	Unit	Condition
V_{SAT}	Saturation Output Voltage	200	700		mVp-p	Note 8
DR	Dynamic Range		1000			See definition of terms
SE	Saturation Exposure		0.28		$\mu J/cm^2$	Note 6
R	Responsivity		2.5		$V/\mu Jcm^{-2}$	Note 6
Z	Output Impedance		1000		ohm	
CTF_H	Contrast Transfer Function, Horizontal		75		%	At 190/380 line pairs/ picture width
CTF_V	Contrast Transfer Function, Vertical		70		%	At 244/488 line pairs/ picture height
DSSNU	Dark Signal Shading		1	10	% V_{SAT}	Measured with a 1.5 kHz cutoff low pass filter. Note 8, 9
PRSNU	Photo Response Shading		1	10	% V_{OUT}	Measured at V_{OUT} = 50% V_{SAT} with a 1.5 kHz low pass filter. Note 8

Notes

1. Adjustment is required within the indicated range for optimum operation.
2. $C_{\phi P} \approx$ 4,000 pF for CCD211; $C_{\phi P} \approx$ 16,000 pF for CCD221.
3. $C_{\phi H1} = C_{\phi H2} \approx$ 100 pF for CCD211; $C_{\phi H1} = C_{\phi H2} \approx$ 200 pF for CCD221.
4. $C_{\phi V1} = C_{\phi V2} \approx$ 3,000 pF for CCD211; $C_{\phi V1} = C_{\phi V2} \approx$ 12,000 pF for CCD221.
5. Devices are tested at a clock rate of 7.2 MHz. This gives a standard NTSC rate at 30 frames per second. Higher clock rates are possible. Operation of the device at lower or higher frequencies will not damage the device. Two factors contribute to the fundamental low frequency limit: dark current contributions from the photosites and associated dark current non-uniformities, and dark current contributions in the register which will result in increased average dark signal at the output. The longer the intergration time, the higher the spatial non-uniformities.
6. 1 $\mu J/cm^2$ = (1 μW – S)/cm^2
   1 $\mu W/cm^2$ = 3.5 lux with 2854°K + BG-38 filter.
   1 lux = 0.03 $\mu W/cm^2$ with 2854°K + BG-38 filter.
   Energy is measured *after* the filter.
7. Measured with a 100% contrast bar pattern as a test target. The saturation level is where the video peaks just start to flatten out as the incident illumination is increased.
8. Measurement excludes single point blemishes, line and column defects and outer edge elements on a line or field basis.
9. DSSNU reduces (increases) in magnitude by a factor of 2X for every 7-10° reduction (increment) in chip temperature.
10. Minimum increase DSNU for certain arrays results when the low level for these clock signals is between 0 and – 6V with respect to V_{SS}.

Cosmetic Performance Specifications

The CCD211 and CCD221 are each available in three cosmetic quality grades. The CCD211A/CCD221A are very high performance devices which are intended for use in the most demanding industrial and scientific applications. The CCD211B/CCD221B are medium grade devices which can be used in situations where a small number of cosmetic defects can be tolerated. The CCD211C/CCD221C are cost-effective devices intended for those applications where less stringent blemish criteria are permissible, for example, in systems which employ computer-based circuitry for analysis of sensor data.

A CCD211 or CCD221 element is considered to be blemished if it exhibits a spurious output (in comparison to its nearest neighbors) of more than 10% of V_{SAT}. Blemish content is determined in the dark, and at an illumination level of 50% V_{SAT}. Single Point Blemishes (SPB's) and column-oriented blemishes (vertical lines) are sometimes found in CCD211 and CCD221 sensors; horizontal line defects are rarely found because of Fairchild's choice of device structure. SPB and column defect locations are random in the CCD211 and CCD221.

Blemish Specifications for CCD211:

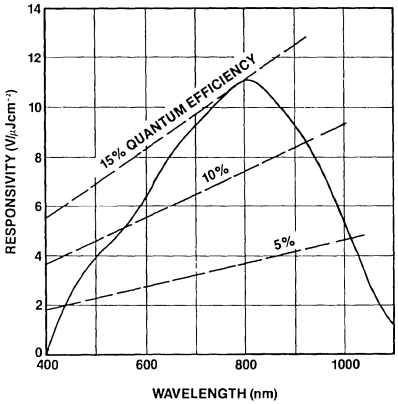
	CCD211A Max	CCD211B Max	CCD211C Max	
Number of Single Point Blemishes (SPB)	10	20	50	
Largest SPB Dimension	3	5	8	contiguous pixels
Number of Column Defects (CD)	0	1	4	
Widest Column Defect Width	0	2	3	adjacent columns

Blemish Specifications for CCD221:

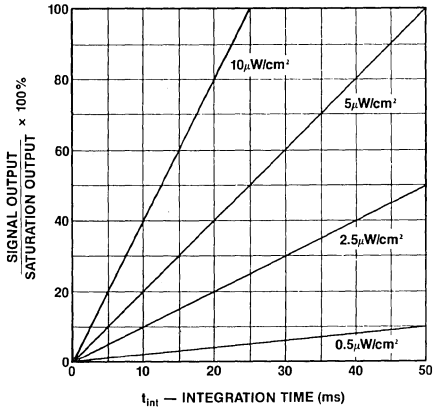
	CCD221A Max	CCD221B Max	CCD221C Max	
Number of Single Point Blemishes	100	200	300	
Largest SPB Dimension	3	5	8	contiguous pixels
Number of Column Defects	4	6	10	
Widest Column Defect Width	2	3	4	adjacent columns
Number of Short Column Defects (SCD)	0	1	2	
Longest SCD Length	0	32	100	lines
Widest SCD Width	0	4	8	columns

Typical Performance Curves

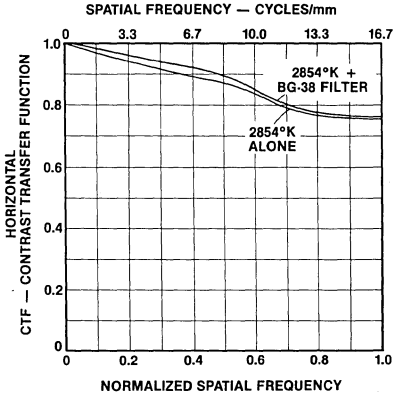
TYPICAL SPECTRAL RESPONSE



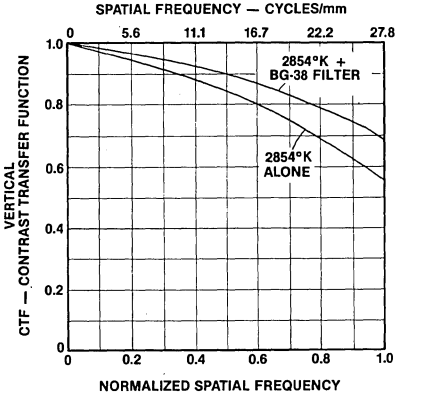
OUTPUT SIGNAL LEVEL VERSUS
INTEGRATION TIME 2854°K TUNGSTEN
SOURCE WITH SCHOTT BG-38 FILTERS



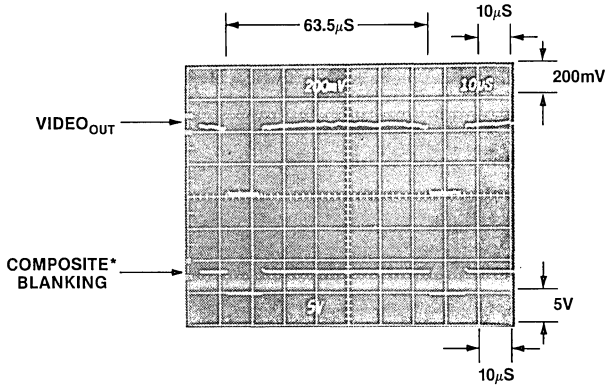
HORIZONTAL CONTRAST
TRANSFER FUNCTION FOR TWO
BROADBAND ILLUMINATION SOURCES



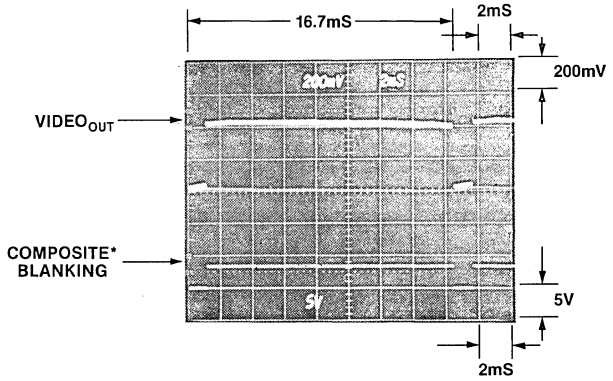
VERTICAL CONTRAST
TRANSFER FUNCTION FOR TWO
BROADBAND ILLUMINATION SOURCES



Output Waveform ($VIDEO_{OUT}$) Under Uniform Illumination (≈ 50% V_{SAT})
Example Shown is for CCD 221



ONE HORIZONTAL LINE

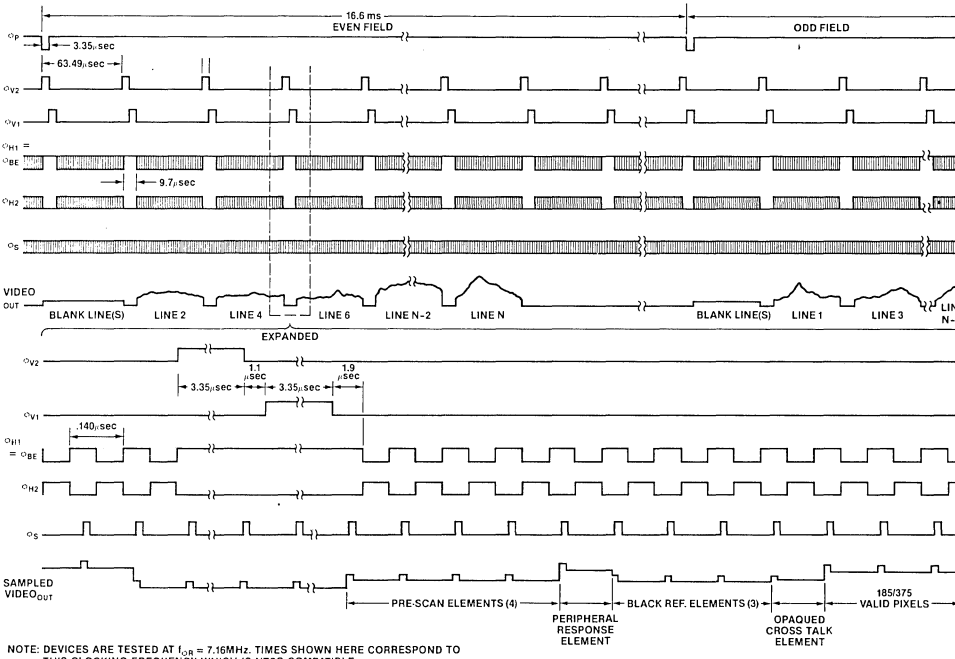


ONE VERTICAL FIELD

*COMPOSITE BLANKING IS GENERATED
IN CAMERAS CCD2000C AND CCD2100C

CCD211/CCD221

Timing Diagram
CCD211: N = 244
CCD221: N = 488



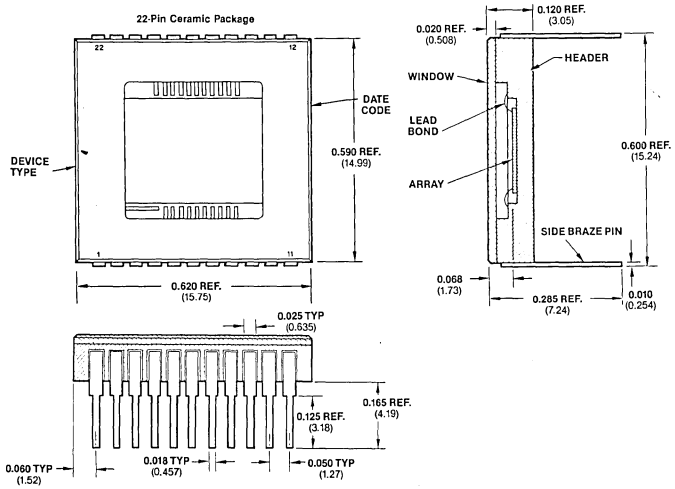
NOTE: DEVICES ARE TESTED AT f_{CR} = 7.16MHz. TIMES SHOWN HERE CORRESPOND TO THIS CLOCKING FREQUENCY WHICH IS NTSC COMPATIBLE.

Order Information
To order the CCD211 or CCD221, please follow the ordering codes listed in the table below:

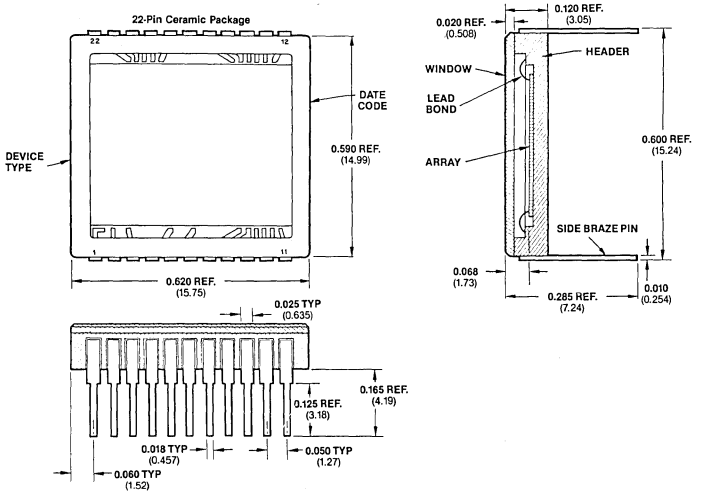
Description	Device Type Order Code
CCD211 Class A Blemish Spec	CD211ADC
CCD211 Class B Blemish Spec	CD211BDC
CCD211 Class C Blemish Spec	CD211CDC
CCD221 Class A Blemish Spec	CD221ADC
CCD221 Class B Blemish Spec	CD221BDC
CCD221 Class C Blemish Spec	CD221CDC

For further information, please call your nearest Fairchild Sales Office. For technical assistance, call (415) 493-8001.

CCD211 Package Outline



CCD221 Package Outline



NOTES: All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Glass window is attached to header with epoxy cement.