7-1. INTRODUCTION

This section contains functional descriptions of the accessory units and plug-in modules that are available for use in the LDH-1/00S Camera Head. Photographs or pw layouts, block diagrams and schematics for these modules are located in Section 5.

7-2. RGB OUTPUT MODULE

The RGB Output Module is designed to provide separate RGB video outputs. The module is provided with three coaxial connectors on the front panel with the following functions:

CONNECTOR	SIGNAL
R	Red video (1V p-p)
G+S	Green video with sync pulses (1.4V p-p)
B	Blue video (1V p-p)

The RGB picture or waveform monitor may be connected to the RGB Output Module using these connectors. If the monitor has a separate sync input, the G + S signal must be looped through the green video input of the monitor and connected to the sync input. The sync pulse amplitude on connector G + S is adjustable with SYNC AMPL control (R45) (0.3V or 0.4V p-p). The contour signal is added to the three video output signals. All unused loop-through inputs must be terminated with 75 ohms.

Circuit Description (Figure 5-2)

RGB video output signals from the Camera Video Board enter on pins 21, 20 and 18 and are fed to common collector circuits (TS1, TS4 and TS7). The contour signal derived from the Video Board enters on pin 15 and is fed through common collector circuit (TS14). The contour signal is then added to the red, green and blue video signals via amplifiers (TS10, TS11 and TS13), respectively. The sync signal from the sync pulse generator enters pin 16 and is fed to amplifier (TS15). The sync pulse is shaped by R35 and C7, amplified by (TS12) and added to the green video signal. The RGB video signals are amplified by (TS2-3, TS5-6 and TS8-9), respectively and are fed to the output connectors on the module front panel. In the Systems Compatible Camera Version the RGB video signals are also fed to camera cable connector (Z) and are available at the Remote Control Unit rear panel.

7-3. ENCODER MODULES (NTSC AND FCC/NTSC)

The Encoder Module is designed to provide a video signal or a composite signal output. The module has two coaxial connectors on the front panel as follows:

CONNECTOR	SIGNAL
VHF	Video modulated RF signal
CVBS	Composite signal

The VHF connector provides a video modulated RF output signal to drive a television receiver for closed circuit applications. The CVBS (composite video, blanking, sync) connector provides a standard FCC color output signal suitable for broadcast transmission.

Circuit Description (Figure 5-5)

RGB video output signals from the Video Board enter on Pins 21, 20 and 18 and are fed to the matrix (TS1-TS5). The outputs of the matrix are: the luminance signal (Y) which is fed to the amplifier (TS6); the B-Y signal which is fed through the amplifier (TS26) and low pass filter (L8-9) to the input of the common collector circuit (TS27); the R-Y signal which is fed through the amplifier (TS37) and low pass filter (L12-13) to the input of the common collector circuit (TS38). [In the FCC/NTSC encoder the R-Y and B-Y signals are applied to the inputs of the common collector circuits (TS51, TS52) from which they are fed through the filter (TS26, TS50) to the input of the common collector circuit (TS27) as a Q signal and through the filter and delay (TS37) to the input of the common collector circuit (TS38).]

The 3.58MHz subcarrier signal from the Subcarrier module enters on Pin 9 and is fed through phase shift networks to the balanced common collector circuit (TS33-34) and through the balanced collector circuit (TS35-36) to the PAL switch (TS48-49). The subcarrier signals at the output of the balanced common collector circuits (TS33-34) leads the signal at the output of the PAL switch (TS48-49) by 90^{o}.

The contour signal from the Video Board enters on Pin 15 and is fed to the common collector circuit (TS18). Sync from the pulse board enters on Pin 16 and is fed to the sync restorer (TS17). The output of the sync restorer is added to the contour signal output from the common collector circuit (TS18) and fed to the amplifier (TS7). [In the FCC/NTSC encoder, blanking from the pulse board enters on Pin 4 and is fed to the amplifier (TS39). The blanking output from this amplifier is added to the sync and contour signals to provide set-up which is adjustable by R203. This added signal is then fed to the amplifier (TS7).] A second output of the sync restorer is fed to the clamp pulse generator (TS21-25) where clamp pulses are formed and fed to the clamp circuits (TS45-47).

7-3. ENCODER MODULES (Continued)

The signal output of amplifier (TS7) is added to the luminance (Y) signal at the output of amplifier (TS6) and fed to the delay line (L16) where it is delayed 600ns and fed to common collector circuit (TS8). The output of this stage is fed through the notch filter, which may be by-passed by switch (TS44) to common collector circuit (TS9). The output of this stage is clamped by clamp circuit (TS45) and fed to common collector circuit (TS10).

The B-Y [Q] signal at the output of the common collector circuit (TS27) is clamped by clamp circuit (TS46) and is fed through the driver carrier balance stage (TS28) to the B-Y [Q] modulator (TS29-30, GR3-6) where it is modulated by the subcarrier signal with the 90° leading phase. The R-Y [I] signal at the output of common collector circuit (TS38) is clamped by clamp circuit (TS47) and fed through the driver carrier balance stage (TS41) to the R-Y [I] modulator (TS42-43, GR9-12) where it is modulated by the subcarrier signal with the 0° phase. The outputs of the B-Y [Q] and R-Y [I] modulators are added and fed through the band-pass filter (L10-11) to the amplifier (TS31-32). The output signal is added to the luminance signal at the output of common collector circuit (TS10) and fed to the output stage (TS11-12) which feeds the output connector (CVBS).

A second output from the output stage is fed to the AM modulator (GR1-2, TS14-15). A program audio signal from the VSA Unit enters on Pin 5 and is fed through amplifier (TS13) to the AM modulator. The video and audio signals are modulated by the RF signal from VHF oscillator (TS16) and the modulated output signals are fed to the output connector (HF).

Adjustments

With RGB video inputs from a color bar generator at 75% color saturation (1.5V p-p input), the following controls may be adjusted to obtain a standard encoded color bar signal:

CONTROL	FUNCTION
Y Amplitude (R26)	Varies first step (white) from 75 to 90 units. Set at 77 units.
Sync Amplitude (R85)	Varies sync from 0 to -60 units. Set at -40 units.
Burst Amplitude (R95)	Varies burst from 0 to $\pm$35 units. Set at $\pm$20 units.
$\Delta\phi$ (R92)	Varies burst phase approx. 3°; used to compensate for phase error due to component tolerances.

7-3. ENCODER MODULES (Continued)

CONTROL	FUNCTION
Set-up Amplitude (R203)	Varies set-up from 0 to 22 units. Set at 10 units.
Carrier Balance (R118, R179)	Adjust to obtain minimum subcarrier (< 15MV) in base line.
Chroma Amplitude (R135)	Varies chroma amplitude of bars; third (Cyan) bar varies from (45 to 90) units to (0 to 15) units. Set at (14 to 100) units.
Q Amplitude (R126)	Varies amplitude of Q channel modulation; second (Yellow) bar varies from (42 to 98) units to (38 to 102) units. Set at (40 to 100) units.
+45° (Q Phase) (R139)	Varies phase of Q signal from 85° to 95° with respect to I signal. Set at 90° with respect to I signal. Using encoded standard color bar adjust so that top of second bar (Yellow) is at 100 units and bottom of seventh bar (Blue) is at -13 units.

Technical Summary

The power requirements and input/output signal levels for the Encoded Modules are outlined as follows:

Power Input:	+6.3Vdc	8.4MA	(Pin 6)
	-12Vdc	88MA	(Pin 11)
	+12Vdc	190MA	(Pin 12)

Signal Input:

Composite Blanking	5V p-p neg from Pulse module (Pin 4).
Audio Subcarrier	See VSA Unit spec. (Pin 5).
Subcarrier	5V p-p from Subcarrier module (Pin 9).
Burst Key	2V p-p neg from Subcarrier module (Pin 14).
Contour	0-1.0V p-p adj. from video board (Pin 15).
Sync	5V p-p neg from Pulse module (Pin 16).
Blue Video	2V p-p adj. from video board (Pin 18).
Green Video	2V p-p adj. from video board (Pin 20).
Red Video	2V p-p adj. from video board (Pin 21).

Signal Output:

CVBS	1V p-p composite signal into 75 ohms; (BNC connector on front panel).
VHF	1mV across 75 ohms; modulated with CVBS video signal (BNC connector on front panel).

7-4. PULSE (PULSE GEN SYNC LOCK) MODULES

The Pulse Module provides horizontal drive, vertical drive, sync and blanking signals for the camera system. It works in conjunction with the Subcarrier Module to provide the signals necessary to produce a color video signal.

The Pulse Gen Sync Lock Module provides horizontal drive, vertical drive, sync and blanking signals for the camera system. It works in conjunction with the Subcarrier Sync Lock Module to lock the camera to an external sync generator when both external sync and subcarrier input signals are provided to the camera.

Circuit Description (Figure 5-10)

The Pulse Module and Pulse Sync Lock Module are identical except for the addition of the vertical phase lock circuitry (as shown in dotted lines in the block diagram, Figure 5-10) in the Pulse Sync Lock Module.

The master oscillator (TS1, 2, 3) is a crystal controlled oscillator operating at a frequency of 251.748KHz. This frequency is controlled by the AFC voltage from the Subcarrier Module to lock it to the subcarrier frequency. The output of the master oscillator is fed through a buffer amplifier (TS4) to a divide-by-eight counter (IC1, P/O IC2) where the frequency is divided down to twice the horizontal frequency. The output of the divide-by-eight counter is fed through a buffer amplifier (TS11) to the serration shaper (TS14) which provides the correct width serration pulses; a divide-by-two counter (P/O IC2) which divides the frequency down to the horizontal frequency; and the delay amplifier (TS12) which delays the pulses the width of the serrations minus the width of the front porch.

The output of the delay amplifier drives the equalizing shaper (TS15) which provides the correct width equalizing pulses; a series of counters (divide-by-three [IC4]; divide-by-seven [IC5, IC6]; divide-by-five [IC7, P/O IC8] and divide-by-five [P/O IC8, IC9] which divides the frequency down to the vertical range; and the emitter follower (TS13) which drives the flip-flop (P/O IC3). This flip-flop is also triggered by the output of the divide-by-two counter and provides a square wave output at horizontal frequency through the buffer amplifier (TS16) to the horizontal blanking shaper (TS19); horizontal sync shaper (TS17); and horizontal drive shaper (TS18). The divide-by-two counter also drives a second divide-by-two counter (P/O IC3) which feeds an output at half the horizontal frequency to pin 5. The output of the horizontal drive shaper is fed through an inverter (P/O IC11) to the output amplifier (TS9) which feeds a negative horizontal drive output to pin 19. The buffer amplifier (TS16) also feeds a horizontal square wave output to pin 15.

7-4. PULSE MODULES (Continued)

The three-input gate (P/O IC14) receives inputs from the first and second divide-by-five counters and provides a positive vertical blanking pulse which is fed to the two-input gate (P/O IC14) where it is mixed with the horizontal blanking from the horizontal blanking shaper and fed to the output amplifier (TS5, TS6) which provides negative mixed blanking output to pins 13 and 14.

The two-input gate (P/O IC11) receives inputs from the divide-by-seven counter and provides an output of a series of negative pulses having a width of nine horizontal lines. These pulses are fed to a three-input gate (P/O IC13) where they are gated with a signal from the first divide-by-five counter and the vertical blanking pulse from the inverter (P/O IC14). The output of the gate is a positive pulse at the vertical frequency having a width of nine horizontal lines. This pulse is fed to two inverters (P/O IC13). One of these inverters is fed to a third inverter (P/O IC13) and to a three-input gate (P/O IC12) where it is gated with two inputs from the divide-by-seven counter to provide a positive pulse at the vertical frequency having a width of three horizontal lines. The output of this gate is fed to another three-input gate (P/O IC12) whose other inputs are the nine line pulse from the second inverter to which has been added the horizontal sync pulses from the horizontal sync shaper and the nine line pulse from the third inverter to which has been added the equalizing pulses from the equalizing pulse shaper. The output of this gate is a negative sync signal minus the serrations during the vertical interval and with no front porch subtracted from the leading edge of the horizontal sync pulses. This signal is fed to a two-input gate (P/O IC11) where it is gated with the serration pulses from the serration shaper to subtract out the serrations during the vertical interval and the front porch from the horizontal sync. The output of this gate is positive composite sync which is fed through an inverter (P/O IC11) to the output amplifier (TS7, TS8) which provides negative composite sync outputs to pins 16 and 17.

A two-input gate (P/O IC15) receives input signals from the divide-by-seven counter. The output of this gate is a series of negative pulses with a width of six horizontal lines. The output of this gate is fed to a second two-input gate (P/O IC15) where it is gated with a pulse at the vertical frequency having a width of nine horizontal lines. This input is also fed as a negative pulse output to pin 20. The output of the gate is a positive vertical drive pulse which is fed through the inverter (P/O IC15) to the output amplifier (TS10) which provides negative vertical drive to pin 21.

In the Pulse Sync Lock Module, the vertical phase lock circuitry (as shown in dotted lines) is connected between TS12 and IC4. The pulse signals from TS12 pass normally through the pulse adder gate (P/O IC 20) and on to IC4. When external sync and subcarrier signals are connected to the camera, voltage is applied to the vertical phase lock circuitry, and a vertical reference signal derived from the external sync is fed to the single shot multivibrator (IC21). A signal at the vertical frequency of the pulse board is

7-4. PULSE MODULES (Continued)

fed from the second divide-by-five counter to the shaper (TS20) and the inverter (P/O IC20) which drives a single shot multivibrator (IC16). The output of this single shot multivibrator is fed to one side of the two flip-flops (IC19) to turn their outputs to the off condition and to the flip-flop (P/O IC17). The other input to this flip-flop comes from the shaper. The two outputs from this flip-flop are fed to the two three-input gates (P/O 17) where they are gated with the output from the shaper and the output from the single shot multivibrator triggered by the external vertical reference. If the internal and external vertical signal are out of phase, a signal will appear at one or the other of the gates depending on whether the internal vertical signal leads or lags the external vertical signal. The signal at the gate output will turn on the appropriate flip-flop (IC19) which will apply a signal through its shaper (TS21 or TS22) to the pulse adder gate (P/O IC20) to add or subtract pulses to or from the pulse train being fed to the counters, thereby causing the internal vertical signal to advance or retard until it becomes locked in phase with the external vertical signal.

Technical Summary

The power requirements and input/output signal levels for the Pulse Module and Pulse Gen Sync Lock Module are outlined as follows:

Power Input

+6.3Vdc	120MA	(Pin 6)
-12Vdc	7.6MA	(Pin 11)
+12Vdc	7.6MA	(Pin 12)

Signal Input

AFC Voltage	+2 to -12Vdc from Subcarrier Sync Lock (Pin 2).
+6.3Vdc Switched*	From Subcarrier Sync Lock when in External Mode (Pin 7).
Vert. Reference*	6V p-p neg from Subcarrier Sync Lock when in External Mode (Pin 18).

Signal Output (when connected in operating camera)

1/2fH Square Wave	6V p-p (Pin 5).
Composite Blanking	4.5V p-p neg (Pin 13, 14).
Horiz. Square Wave	6V p-p (Pin 15).
Composite Sync	5V p-p neg (Pin 16, 17).
Horiz. Drive	6V p-p neg (Pin 19).
Burst Key Out Pulse	5V p-p neg (Pin 20).
Vert. Drive	6V p-p neg (Pin 21).

Internal Controls

Master Oscillator Frequency (C7)	With -4Vdc applied to Pin 2, master oscillator frequency range with adjustment of C7 is from 251.732KHz to 251.780KHz. Adjust C7 for 251.748KHz.

* Pulse Gen Sync Lock Only.

7-5. EXTERNAL PULSE MODULE

The External Pulse Module accepts horizontal drive, vertical drive, blanking and sync from an external sync generator and provides the necessary sync, blanking and drive pulses to operate the camera system. The module has four coaxial input connectors on the front panel as follows:

CONNECTOR	SIGNAL
J1	Horizontal Drive
J2	Vertical Drive
J3	Blanking
J4	Sync

Circuit Description (See Figure 5-15)

All four input signals are processed in the same manner. The signal enters an inverter stage and is then fed to a differential amplifier. The amplified output is fed to a phase splitter circuit that provides two signals 180° out of phase. These signals drive the bases of the two transistors in the output amplifier stage.

Technical Summary

The power requirements and input/output signal levels for the External Pulse Module are outlined as follows:

Power Input

+6.3Vdc	21.2MA	(Pin 6)
-12Vdc	55MA	(Pin 11)
+12Vdc	27.6MA	(Pin 12)

Signal Input

Horiz. Drive	4V p-p neg into 75 ohm termination from External Sync Generator (J1).
Vert. Drive	4V p-p neg into 75 ohm termination from External Sync Generator (J2).
Blanking	4V p-p neg into 75 ohm termination from External Sync Generator (J3).
Sync	4V p-p neg into 75 ohm termination from External Sync Generator (J4).

Signal Output (when connected in operating camera)

Horiz. Drive	3V p-p neg (Pin 15, 19)
Vert. Drive	3V p-p neg (Pin 21)
Blanking	3V p-p neg (Pin 13, 14)
Sync	3V p-p neg (Pin 16, 17)

7-6. SUBCARRIER (SUBCARRIER SYNC LOCK) MODULES

The Subcarrier Module provides the subcarrier signal (3.58MHz) and AFC voltage for the camera system. It works in conjunction with the Pulse Module to provide the signals necessary to produce a color video signal.

The Subcarrier Sync Lock Module provides the subcarrier signal, AFC voltage and burst key for the camera system. It works in conjunction with the Pulse Sync Lock Module to lock the camera to an external sync generator when both external sync and subcarrier input signals are provided to the camera.

Circuit Description (Subcarrier Module, see Figure 5-18)

The Subcarrier oscillator (TS1, TS2) is a crystal controlled oscillator which is adjusted with C5 to oscillate at a frequency of 3.579545MHz. The transformer (T1) is adjusted to couple the maximum amplitude sinewave into balanced emitter followers (TS3, TS4). The output of the balanced emitter followers is fed to the output (Pin 9) and through a second set of balanced emitter followers (TS5, TS6) to discriminator (GR1-GR4). A signal at half the horizontal frequency is fed to blocking oscillator (TS7). The output of the blocking oscillator, consisting of two pulses 180^{o} out of phase at half the horizontal frequency, is fed to the discriminator. The discriminator output is a voltage proportional to the difference between the subcarrier oscillator frequency and that of the master oscillator on the Pulse Module. This voltage is fed through the low pass filter (C18, C28, C29, R44, R45) to the DC amplifier (TS14, TS15, TS16) where it is amplified and fed to the AFC voltage output (Pin 2).

A horizontal square wave (H') is applied to burst keying generator (TS8, TS9, TS12) where it is delayed and shaped to form the burst key pulse. A vertical pulse is fed through the suppression circuit (TS10, TS11) to the burst keying generator to suppress the burst key pulse during the vertical sync interval. The burst key pulse is fed through emitter follower (TS13) to the output (Pin 14).

Circuit Description (Subcarrier Sync Lock Module, see Figure 5-21)

On the Subcarrier Sync Lock Module the generation of the burst key pulse is the same as on the Subcarrier Module except that provisions are made to adjust the start of the burst key pulse (R100) and the pulse width (R101).

In the internal mode of operation (when both external sync and external subcarrier signals are not present) supply voltages are applied to the internal circuitry as shown in the block diagram (Figure 5-21) and operation of the subcarrier and AFC circuits

7-6. SUBCARRIER MODULES (Continued)

are as described for the Subcarrier Module with the following exceptions: the AFC output voltage is fed from DC amplifier (TS14, TS15, TS16) through diode gate (GR15) to the output (Pin 2). The subcarrier signal from balanced emitter followers (TS3, TS4) is fed through diode gate (GR1, GR2) to the tuned amplifier (P/O IC1). The diodes (GR3, GR4) in the output of the emitter followers provide a current source to the emitter input of the AGC amplifier. The output of the AGC amplifier drives phase shift amplifier (IC2, TS1). The outputs of the phase shift amplifier are used to drive a series of differential amplifiers (IC3, P/O IC4) with the signal shifted in phase as shown in the block diagram (Figure 5-21). In the differential amplifiers the input from the preceding stage is held at a fixed bias and the input with the leading phase has its bias varied by adjusting R96. As the bias is increased, the output of each differential amplifier will be shifted in phase as shown in the block diagram (Figure 5-21) due to the addition of the signal currents in the emitters of the differential pair. The output of the fourth differential amplifier is a subcarrier signal which can be shifted in phase from 0-360^{o} by adjusting R96. This signal is amplified by tuned amplifier (P/O IC4) and fed through emitter followers (P/O IC4, TS2) to the output (Pin 9). The output signal amplitude is detected by AGC detector (GR5, GR6) and fed back as a DC voltage to the AGC amplifier to keep the output signal amplitude constant.

In the external mode of operation (when both external subcarrier and external sync are present) the incoming subcarrier signal is amplified in amplifier (P/O IC1) and detected by detector (P/O IC2) to provide a positive DC voltage to one input of gate (P/O IC2). The incoming sync signal is amplified by amplifier (P/O IC1) and detected by detector (P/O IC2) to provide a positive DC voltage to the second input of the gate (P/O IC2). When both of these signals are present the gate output drops to zero which triggers switch (TS18) applying the 6.3V switched to the following circuits: those shown on the block diagram (Figure 5-21); the output (Pin 7); and the switch (TS17, K1) which switches the +12V and -12V supplies from the internal to the external circuitry as shown.

When the internal subcarrier is turned off, the external subcarrier signal from amplifier (P/O IC1) passes through diode gate (GR1, GR2) and is processed by the phase shift circuitry as described previously in the internal operation mode.

The external sync signal is fed from the output of amplifier (P/O IC1) to a single-shot multivibrator (IC5); a gate (P/O IC2) and a second single-shot multivibrator (IC3). The output of single-shot multivibrator (IC5) is also fed to gate (P/O IC2) whose output is the vertical reference signal to Pin 18. The second single-shot multivibrator (IC3) drives a third single-shot multivibrator (IC4) whose output pulse width can be varied by adjusting R79. This adjustment allows the phase of the horizontal pulses generated by

7-6. SUBCARRIER MODULES (Continued)

the pulse board to be varied over a sufficient range to compensate for the delay in the external horizontal sync due to long cable lengths. The output of this third single-shot multivibrator drives a paraphase amplifier (TS21, TS22) which generates two pulses, 180° out of phase, which are applied to discriminator (GR11-GR14) where they are compared with the horizontal square wave (H') from the amplifier (P/O IC1, TS20). The output of the discriminator is a DC voltage proportional to the difference between the external horizontal sync frequency and the frequency of the horizontal pulses generated in the Pulse Sync Lock Module. This voltage is fed through the low pass filter (C47, C51, R92) to the DC amplifier (IC6) where it is amplified and fed through diode gate (GR15) to the AFC voltage output (Pin 2).

Technical Summary

The power requirements, input/output signal levels and adjustments for the Subcarrier Module and Subcarrier Sync Lock Module are outlined as follows:

Power Input

	Internal Mode	External Mode
+6.3Vdc	42MA	115MA (Pin 6)
-12Vdc	92MA	64MA (Pin 11)
+12Vdc	115MA	110MA (Pin 12)

Signal Input

1/2fH	6V p-p from Pulse Sync Lock (Pin 5).
Horiz. Square Wave (H')	6V p-p from Pulse Sync Lock (Pin 15).
Vert. Pulse	5V p-p neg from Pulse Sync Lock (Pin 20).
Ext. Sync *	4V p-p neg (1V p-p min.) into 75 ohm termination from External Sync Generator (Pin 16).
Ext. Subcarrier *	2V p-p (0.5V p-p min.) into 75 ohm termination from External Sync Generator (Pin 19).

Signal Output (when connected in operating camera)

AFC Voltage	+2 to -12Vdc (Pin 2).
Subcarrier	5V p-p (Pin 9).
Burst Key	2V p-p neg (Pin 14).
6.3Vdc Switched *	When both Ext. Sync and Subcarrier are present (Pin 7).
Vert. Reference *	6V p-p neg when both Ext. Sync and Subcarrier are present (Pin 18).

* Subcarrier Sync Lock Only.

7-6. SUBCARRIER MODULES (Continued)

External Controls

Horizontal Phase (R79)	Various horizontal pulses from -18 to +9 microseconds with respect to External Horizontal Sync Pulse. Set to required delay for cable length used by observing both External Horizontal Sync and Composite Sync Signal Output on dual trace oscilloscope and adjusting R79 so that both sync signals are in phase.
Subcarrier Phase (R96)	Varies Subcarrier phase from 0° to 360° with respect to External Subcarrier. Set to required phase shift to match other video sources at switcher location.

Internal Controls

Burst Pulse Start (R100)	Varies start of burst from +0.2 to +2.2 microseconds with respect to end of sync set to 0.56µsec; +0.08, -0.17µsec.
Burst Pulse Width (R101)	Varies number of cycles in burst from 7 to 10 cycles. Set for 8 full cycles.
Internal Subcarrier Frequency (C5)	Varies frequency of Internal Subcarrier Oscillator from 3.578500 MHz to 3.580250 MHz. Adjust C5 for 3.579545 MHz.
Internal Subcarrier Amplitude (T1)	Varies amplitude of Internal Subcarrier at E1 from 0.4 to 6V p-p set to maximum.

7-7. EXTERNAL SUBCARRIER MODULE

The External Subcarrier Module accepts subcarrier and burst key (burst flag) signals from an external sync generator and provides the necessary subcarrier (3.58MHz) and burst key signals to operate the camera.

Circuit Description (see Figure 5-24)

The external subcarrier input signal (3.58MHz) enters J1 and is fed to tuned amplifier (TS4). The output of this amplifier is fed through emitter followers (TS5, TS6) to AGC amplifier (TS7, TS9). The diode bridge (GR1-GR4) in the output of the emitter follower stage provides a current source to the emitter input of the AGC amplifier. The output of the AGC amplifier drives phase shift amplifier (TS12-TS16). The outputs of the phase shift amplifier are used to drive a series of differential amplifiers (TS17-TS20) with the signal shifted in phase as shown in the block diagram (Figure 5-24). In the differential amplifiers, the input from the preceding stage is held at a fixed bias and the input with the leading phase has its bias varied by adjusting R111. As the bias is increased, the output of each differential amplifier will be shifted in phase as shown in the block diagram (Figure 5-24), due to the addition of signal currents in the emitters of the differential pair. The output of the fourth differential amplifier is a subcarrier signal which can be shifted in phase from 0-360° by adjusting R111. This signal is amplified by tuned amplifier (TS22) and fed through emitter followers (TS23, TS24) to the output (Pin 9). The output signal amplitude is detected by AGC detector (GR5, GR6) and fed back as a DC voltage to the AGC amplifier to keep the output signal amplitude constant.

The burst key signal from the external subcarrier generator enters J2 and is fed to an inverter stage (TS29). The inverted output drives differential amplifier (TS25, TS26). The amplified output is fed to a phase splitter circuit (TS27) that provides two signals 180° out of phase. These signals drive the bases of the output amplifier transistors (TS28, TS30).

Technical Summary

The power requirements, input/output signal levels and adjustments for the External Subcarrier Module are outlined as follows:

Power Input

+6.3Vdc	4.5MA	(Pin 6)
-12Vdc	60MA	(Pin 11)
+12Vdc	96MA	(Pin 12)

7-7. EXTERNAL SUBCARRIER MODULE (Continued)

Signal Input

Subcarrier	2V p-p into 75-ohm termination from External Sync Generator (J1).
Burst Key	4V p-p negative into 75-ohm termination from External Sync Generator (J2).

Signal Output (when connected in operating camera)

Subcarrier	3V p-p (Pin 9)
Burst Key	3V p-p negative (Pin 14)

External Controls

Subcarrier (R111)	Varies Subcarrier phase 0° to 360° with respect to External Subcarrier. Set to required phase shift to match other video sources at video switcher location.